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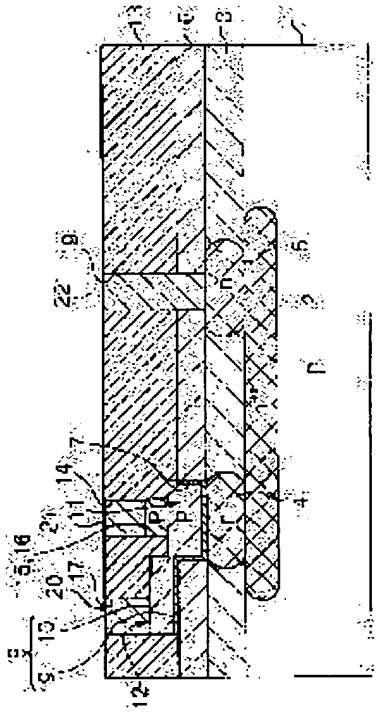
(54) SiGe FILM FORMING METHOD, METHOD OF MANUFACTURING HETEROJUNCTION TRANSISTOR AND HETEROJUNCTION BIPOLAR TRANSISTOR

(57)Abstract:

PROBLEM TO BE SOLVED: To prevent an SiGe film on an insulating film from becoming rough and to improve film quality and film resistance in an SiGe film forming method, a manufacturing method of a heterojunction transistor and a heterojunction bipolar transistor.

SOLUTION: A method for forming a SiGe film 8 on the insulating film 6 is provided with a buffer forming process for forming a first Si(1-x)Gex film 9 ($0 \leq x < 0.05$) on the insulating film and a main film forming process for forming a second Si(1-y)Gey film 10 ($0.05 \leq y < 1$) on the first Si(1-x)Gex film. The buffer forming process forms the first Si(1-x)Gex in the thickness range of 0.5 nm to 5 nm.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the formation approach of the SiGe film and the manufacture approach of a heterojunction transistor suitable as a base outgoing line for example, in a heterojunction transistor, and a heterojunction bipolar transistor.
[0002]
[Description of the Prior Art] By enlarging the band gap of an emitter region and raising emitter injection efficiency sharply rather than a base region, in a low noise and Si, the high-speed operation which cannot be attained is possible for HBT (heterojunction transistor) which aims at increase of current gain, and it is a highly efficient device used for a logical circuit, communication system, microwave devices (amplifier used for A/D conversion), etc.
[0003] Conventionally, although HBT was manufactured by the combination of GaAs and AlGaAs etc., since the band gap of SiGe (silicon-germanium) is smaller than Si (silicon), HBT (SiGe-HBT is called hereafter) using SiGe is developed and studied in recent years. This SiGe-HBT has the advantage of it not being necessary to use As with treatment difficult in environment etc. so much compared with Si in which a manufacturing cost falls compared with the possibility of mixed loading (formation of 1 chip) with abundant Si processes of technical are recording, and Si-LSI which is easy to adjust, and a GaAs device etc.
[0004] As a manufacture process of SiGe-HBT which uses SiGe for a base region, after forming SiO2 on the silicon wafer with which the collector field was formed, preparing base opening (base window part) to this SiO2, growing SiGe epitaxially to this base opening and forming a base region, the emitter region of Si is formed on a base region, for example.
[0005] In addition, in the former, for example, JP,9-181091,A, and JP,2000-31155,A, before performing non-choosing epitaxial growth of SiGe, the technique which forms 10-50nm of Si as a buffer is indicated. moreover, for example D. L.Harame, etc. J(IEEE Transactions on Electron Devices, Vol.42, No., March 1995, p469.).L.Regolini (), etc. [Materials] In Science in Semiconductor Processing The technique of performing non-choosing epitaxial growth of SiGe is proposed without exfoliating a polycrystal Si thin film, after depositing a polycrystal Si thin film all over a wafer and etching the insulator layer of the base section by making this into a mask, in case base opening is processed.
[0006]
[Problem(s) to be Solved by the Invention] However, the following technical problems are left behind in the above-mentioned Prior art. In SiGe-HBT which makes SiGe form with non-choosing epitaxial growth, while the epitaxial layer which grows up to be base opening is used as a base layer (base region), the polycrystal layer which grows on SiO2 succeeding a base layer is used as a base outgoing line. In this case, if direct SiGe is formed on SiO2, resistance of a base outgoing line becomes high considering a film dry area as a lifting and a result, and the polycrystal layer which grows on SiO2 may degrade transistor characteristics. A film dry area tends to produce higher germanium presentation ratio especially required of the base region of HBT, and there is an inclination for the effectiveness to tend to become remarkable, so that thickness is thin.
[0007] With the above-mentioned conventional technique, since 10-50nm of buffer layers of Si is beforehand formed on SiO2, it is thought that it is hard to produce the film dry area of SiGe which

grows on it, but when using this buffer layer as a base layer, base thickness will become thick substantially by 10-50nm of buffer thickness. That is, with the conventional technique, electronic base transit time's having become long, and the merit which adopted the SiGe base layer for high-speed operation having reduced only the part of buffer thickness, and having un-arranged [which becomes slower than the case where the working speed of a transistor forms a base region only by SiGe], although the base layer width of a transistor generally became such a high-speed transistor that it is thin.

[0008] Moreover, although a production process which is different by membrane formation of Polycrystal Si and membrane formation of SiGe is needed with the above-mentioned conventional technique of performing SiGe growth after etching the insulator layer of the base section by using a polycrystal Si thin film as a mask, it is necessary to suppress the heat history in a production process as much as possible, and many [from a viewpoint of the thermal effect to a device / like this conventional technique / as a heat process] is not a desirable thing in LSI manufacture in recent years as a result of detailed wiring.

[0009] This invention aims at offering the formation approach of the SiGe film that it was made in view of the above-mentioned technical problem, it can prevent the SiGe film on an insulator layer being ruined, and membraneous quality and membrane resistance can be improved, the manufacture approach of a heterojunction transistor, and a heterojunction bipolar transistor.

[0010]

[Means for Solving the Problem] As a result of having inquired about the membrane formation technique of SiGe, when this invention persons were germanium presentation ratios of the fixed range, they found out that very thin SiGe buffer thickness could also improve a film dry area and resistance sharply. That is, this invention persons grew the SiGe film into which buffer layer thickness was changed, and measured the resistance while they grew the SiGe film which changed germanium presentation ratio on SiO2 and investigated the membrane formation condition etc. In addition, drawing 5 , drawing 6 , and drawing 7 are the SEM photographs of the SiGe film which carried out germanium presentation ratio to 0.04, and 0.13 and 0.30, respectively. Moreover, drawing 8 is an example of resistance measurement and is a graph which shows the sheet resistance of the SiGe film (the thickness on germanium presentation ratio 0.30 and a buffer layer is the same) at the time of growing up Si film as a buffer layer on SiO2, and changing the thickness of this buffer layer to 0-5nm.

[0011] As drawing 6 - drawing 7 showed, in the case where germanium presentation ratio is 0.13, it turned out that the SiGe film is discontinuity-ized partially, it discontinuity-izes completely in the case of germanium presentation ratio 0.30, and it does not discontinuity-ize on the whole by the case of 0.04 to membranes hardly being formed, but the good membrane formation condition is acquired further. Moreover, as drawing 8 showed, it turned out that resistance is reduced for the thickness of a buffer layer in abbreviation one half by 0.5nm, and resistance falls [thickness] a single figure in 1nm further.

[0012] Therefore, this invention was a technique based on this knowledge, and the following configurations were used for it in order to solve said technical problem. Namely, the formation approach of the SiGe film of this invention The buffer formation process which is the approach of forming the SiGe film on an insulator layer, and forms 1st Si(1-x) Gex film ($0<=x<0.05$) on said insulator layer, It has the main film formation process which forms 2nd Si(1-y) Gey film ($0.05<=y<1$) on said 1st Si(1-x) Gex film, and said buffer formation process is characterized by forming said 1st Si(1-x) Gex film in [0.5nm or more / thickness] 5nm or less.

[0013] Since 1st Si(1-x) Gex film is formed in [0.5nm or more / thickness] 5nm or less, the thick buffer layer of 10-50nm can be made unnecessary like before, discontinuity-ization (film dry area) of the 2nd SiGe film can be improved by the very thin buffer layer, and resistance can also be made to resist sharply in a buffer formation process by the formation approach of this SiGe film. In addition, if 1st Si (1-x) Gex film is set to at least 0.5nm as mentioned above, the effectiveness of reducing resistance sharply rather than the case (only 2nd Si(1-y) Gey film) where 1st Si(1-x) Gex film is not prepared at all will be acquired. For example, even if 2nd Si(1-y) Gey film is germanium presentation ratio y= 0.3, if 1st Si(1-x) Gex film is set to 0.5nm, resistance can be reduced in abbreviation one half, and more preferably if 1nm, single figure resistance can be lowered. In addition, having set 1st Si(1-x) Gex film to 5nm or less has the small effectiveness of the reduction in resistance, even if it thickens more than this, and it is for resistance to seldom change.

[0014] Moreover, at least, the formation approach of the SiGe film of this invention is suitable, when

forming said 2nd Si(1-y) Gey film with the reduced pressure CVD method of 0.133Pa or more pressure range 1.33x104Pa or less. That is, although a reduced pressure CVD method has a possibility that the film dry area of the SiGe film may become remarkable rather than the UHV-CVD method which forms membranes by the high vacuum, it can acquire the effectiveness of film dry-area control notably compared with the growth approaches, such as a UHV-CVD method, by applying a reduced pressure CVD method to the membrane formation approach of 2nd Si(1-y) Gey film of this invention. Moreover, since the good SiGe film can be easily obtained also with a reduced pressure CVD method, the need of using high vacuum techniques, such as a UHV-CVD method, can be lost, and productivity etc. can be raised.

[0015] The manufacture approach of the heterojunction transistor of this invention The process which forms an insulator layer on Si substrate with which it is the approach of manufacturing the heterojunction transistor which has the base region of SiGe, and the collector field was formed, The process which forms in said a part of insulator layer the window part which leads to said collector field, The SiGe film formation process which forms the field with which the outgoing line to a base electrode is presented on said insulator layer while forming the SiGe film in un-choosing on said window part and said insulator layer and forming said base region on a window part, It has the process which forms the emitter region of Si on said base region, and said SiGe film formation process is characterized by forming said SiGe film by the formation approach of the SiGe film of above-mentioned this invention.

[0016] Moreover, the collector field which the heterojunction transistor of this invention is a heterojunction transistor which has the base region of SiGe, and was formed in Si substrate, An insulator layer with the window part which is formed on said Si substrate and leads to said collector field, The base region which is formed on said window part and consists of SiGe film, and the outgoing line which consists of SiGe film which was formed on said insulator layer and connected to said base region, It has the emitter region of Si formed on said base region. At least said outgoing line 1st Si(1-x) Gex film formed on said insulator layer ($0<=x<0.05$), It has 2nd Si(1-y) Gey film ($0.05<=y<1$) formed on said 1st Si(1-x) Gex film, and said 1st Si(1-x) Gex film is characterized by being 0.5nm or more thickness of 5nm or less.

[0017] With the manufacture approach of these heterojunction transistors, and a heterojunction transistor 2nd Si(1-y) Gey film ($0.05<=y<1$) is formed on 1st Si(1-x) Gex film ($0<=x<0.05$), and since 1st Si(1-x) Gex film is 0.5nm or more thickness of 5nm or less Since 1st thin Si(1-x) Gex film is used as the buffer as SiGe film of a base region while the SiGe film with which the film dry area was controlled is obtained and being able to carry out [low ****]-izing of the base outgoing line on an insulator layer, a base layer width can be made thin as a whole.

[0018] Moreover, as for the manufacture approach of the heterojunction transistor of this invention, it is desirable that said SiGe film formation process is [germanium presentation ratio y of said 2nd Si(1-y) Gey film] within the limits of $0.08<=y<=0.3$. Moreover, as for the heterojunction transistor of this invention, it is desirable that germanium presentation ratio y of said 2nd Si(1-y) Gey film is within the limits of $0.08<=y<=0.3$.

[0019] With the manufacture approach of these heterojunction transistors, and a heterojunction transistor, since germanium presentation ratio y of 2nd Si(1-y) Gey film is within the limits of $0.08<=y<=0.3$, a band gap suitable as a base region of HBT is obtained.

[0020]

[Embodiment of the Invention] Hereafter, the formation approach of the SiGe film concerning this invention, the manufacture approach of a heterojunction transistor, and 1 operation gestalt of a heterojunction bipolar transistor are explained, referring to drawing 3 from drawing 1 .

[0021] Drawing 1 shows the rough cross-section structure of the heterojunction bipolar transistor silicon (HBT) of this invention. If the structure of this HBT is explained together with the manufacture process, as shown in (a) of drawing 2 , the pad subcollector field 2 doped by n++ by arsenic placing will be formed in p-type silicon wafer (Si substrate) 1 front face, and the n-Si epitaxial layer 3 of n mold single crystal silicon will be further formed in silicon wafer 1 front face with epitaxial growth.

[0022] Next, as shown in (b) of drawing 2 , the 1st collector well 4 and the 2nd collector well 5 (collector field) which were doped by n+ are generated by Lynn placing so that the pad subcollector field 2 may be arrived at at the n-Si epitaxial layer 3. and it is shown in (c) of drawing 2 -- as -- the front face of the n-Si epitaxial layer 3 -- as an insulator layer -- the 1st SiO two-layer (diacid-ized silicon

layer) -- 6 is formed according to a thermal oxidation process. then, the 1st SiO two-layer -- mask processing is performed to 6, it etches alternatively, and the base window part 7 which leads to the 1st collector well 4 is formed.

[0023] Next, as shown in (d) of drawing 2 , the SiGe film 8 is formed in un-choosing on the base window part 7 and the 1st SiO two-layer 6. This SiGe film 8 has the two-layer structure of the 1st Si(1-x) Gex film (0<=x<0.05) 9 formed as a buffer layer, and the 2nd Si(1-y) Gey film (0.05<=y<1) 10 formed on this 1st Si(1-x) Gex film 9.

[0024] That is, in order to form the SiGe film 8, the 1st Si(1-x) Gex film 9 is first formed with non-choosing epitaxial growth in [0.5nm or more / thickness] 5nm or less on the base window part 7 and the 1st SiO two-layer 6 (buffer formation process). Furthermore, the 2nd Si(1-y) Gey film 10 is formed with non-choosing epitaxial growth on the 1st Si(1-x) Gex film 9.

[0025] In addition, the 1st Si(1-x) Gex film 9 and the 2nd Si(1-y) Gey film 10 form membranes with the reduced pressure CVD method of 0.133Pa or more pressure range 1.33x104Pa or less. Moreover, germanium presentation ratio y of the 2nd Si(1-y) Gey film 10 is more preferably set up within the limits of 0.08<=y<=0.3. Moreover, H2 is used as carrier gas and SiH4 and GeH4 are used for it as source gas while the membrane formation temperature in this reduced pressure CVD method is 600-800 degrees C.

[0026] At this membrane formation process, the 1st Si(1-x) Gex film 9 and the 2nd Si(1-y) Gey film 10 with which the 1st Si(1-x) Gex film 9 and the 2nd Si(1-y) Gey film 10 which are formed in the base window part 7 are formed as an epitaxial layer of a single crystal, and are formed on the 1st SiO two-layer 6 are formed as a non-epitaxial layer of polycrystal. In addition, the 1st Si(1-x) Gex film 9 and the 2nd Si(1-y) Gey film 10 are doped by p by boron. Thus, the base region 11 of the heterojunction by the SiGe film 8 is formed in the base window part 7.

[0027] Next, as mask processing is performed on the 2nd Si(1-y) Gey film 10, it etches alternatively and it is shown in (a) of drawing 3 , it leaves the part with which the base outgoing line 12 and a base region 11 are presented, and the 1st Si(1-x) Gex film 9 and the 2nd Si(1-y) Gey film 10 are removed. furthermore, the exposed 2nd Si(1-y) Gey film [which remained as shown in (b) of drawing 3] 10, and 1st SiO two-layer the 6 top -- the 2nd SiO two-layer -- 13 is formed.

[0028] Next, on the 2nd SiO two-layer 13, mask processing is performed, wet etching is performed alternatively, and the emitter window part 14 which leads to a base region 11 is formed. Then, epitaxial growth of the Si is carried out with a CVD method on the emitter window part 14 and the 2nd SiO two-layer 13, Si single crystal layer 15 is formed to the emitter window part 14, and an emitter region 16 is formed. And mask processing is performed to the emitter window part 14, it leaves the part with which an emitter region 16 is presented, and etching processing removes Si on the 2nd SiO two-layer 13.

[0029] Next, mask processing is performed on the 2nd SiO two-layer 13, wet etching is performed alternatively, and as shown in (c) of drawing 3 , the base-electrode window part 17 which leads to the base outgoing line 12, the emitter electrode window part 18 which leads to an emitter region 16, and the collector-electrode window part 19 which leads to the 2nd collector well 5 are formed. Then, HBT of this operation gestalt is manufactured by embedding a metallic material alternatively at the base-electrode window part 17, the emitter electrode window part 18, and the collector-electrode window part 19, and forming a base electrode 20, the emitter electrode 21, and a collector electrode 22, respectively.

[0030] In the formation approach of the SiGe film of this operation gestalt, the manufacture approach of HBT, and HBT The 2nd Si(1-y) Gey film 10 (0.05<=y<1) is formed on the 1st Si(1-x) Gex film 9 (0<=x<0.05), and since the 1st Si(1-x) Gex film 9 is 0.5nm or more thickness of 5nm or less While the SiGe film 8 with which the film dry area was controlled is obtained and being able to carry out [low ****]-izing of the base outgoing line 12 on the 1st SiO two-layer 6, as SiGe film 8 of a base region 11 Since the 1st thin Si(1-x) Gex film 9 is used as the buffer, a base layer width becomes thin as a whole, and high-speed operation can be obtained.

[0031] Moreover, since the 2nd Si(1-y) Gey film 10 is formed with the reduced pressure CVD method of 0.133Pa or more pressure range 1.33x104Pa or less and the good SiGe film can be easily obtained also with a reduced pressure CVD method while being able to acquire the effectiveness of film dry-area control notably compared with the growth approaches, such as a UHV-CVD method, the need of using high vacuum techniques, such as a UHV-CVD method, can be lost, and productivity etc. can be raised. In addition, since germanium presentation ratio y of the 2nd Si(1-y) Gey film 10 is within the limits of

0.08<=y<=0.3, a band gap suitable as a base region 11 of HBT is obtained.

[0032]

[Example] Next, an example explains concretely the formation approach of the SiGe film concerning this invention, the manufacture approach of a heterojunction transistor, and a heterojunction bipolar transistor.

[0033] 1st Si(1-x) Gex film and 2nd Si(1-y) Gey film were actually formed on SiO two-layer [1st] like the above-mentioned operation gestalt, and the membrane formation condition and resistance (sheet resistance) were investigated. In addition, germanium presentation ratio y of 2nd Si(1-y) Gey film of the example concerning this invention is 0.30. Moreover, thickness is 5nm and, as for 1st Si(1-x) Gex film, germanium presentation ratio uses 0, i.e., Si film.

[0034] Drawing 4 shows the SEM photograph of the SiGe film by the example of this invention. In the case of this example, when this drawing 4 is compared with drawing 7 as an example of a comparison, it turns out that continuation and a good membrane formation condition are acquired to SiGe discontinuity-izing in the case of the example of a comparison which does not have a buffer layer, and membranes hardly being formed.

[0035] Moreover, when the sheet resistance at the time of forming a SiGe layer (germanium presentation ratio 0.30) was investigated, as shown in drawing 8 , to having been 1x105ohms, in the example of this invention, in the case of a SiGe layer without a buffer layer, it is 1x104ohms, and it had also formed a single figure into low resistance. Thus, in the case where this invention is applied, while the good film was obtained compared with the former, large low resistance-ization was obtained.

[0036] In addition, this invention also includes the following operation gestalten. With the above-mentioned operation gestalt, although the formation approach of the SiGe film of this invention was applied to the base outgoing-line formation in HBT, you may apply to manufacture of other devices which have the structure which formed the SiGe film on the insulator layer. For example, in metal-oxide-semiconductor structures, such as an MOS transistor, when forming the SiGe film as a gate electrode on gate oxide, this invention may be applied.

[0037] Moreover, although germanium presentation ratio formed the fixed layer as 1st SiGe film with the above-mentioned operation gestalt, the 1st SiGe film which is changing within the limits of 0<=x<0.05 is sufficient as germanium presentation ratio x. For example, it is contained in this invention, also when the SiGe layer toward which the presentation inclined is formed and germanium presentation ratio x forms the SiGe layer of 0.15 further on the SiGe layer of this inclination presentation, making germanium presentation ratio x increase gradually from 0 to 0.15 on an insulator layer (SiO2).

[0038] That is, if the field of the layer which has early germanium presentation ratio x of 0<=x<0.05 among the inclination presentation SiGe layers formed on an insulator layer is 0.5nm <= 5nm or less in thickness, the field of this layer can regard it as the 1st SiGe film in this invention. And germanium presentation ratio x after this field can consider that the SiGe fields from 0.05 to 0.15 are the 2nd SiGe film in this invention. Thus, the 2nd SiGe film which forms membranes on the 1st SiGe film in this invention also contains the SiGe layer formed continuously, without interrupting a membrane formation process after membrane formation of the 1st SiGe film.

[0039]

[Effect of the Invention] According to this invention, the following effectiveness is done so. Since 1st Si (1-x) Gex film is formed in [0.5nm or more / thickness] 5nm or less in a buffer formation process according to the formation approach of the SiGe film of this invention Make unnecessary the thick buffer layer of 10-50nm like before, and discontinuity-ization (film dry area) of the 2nd SiGe film is improved by the buffer layer of very thin thickness. resistance can also be made to form into low resistance sharply, and can set the SiGe film on an insulator layer to various devices -- low -- it becomes possible to use as wiring [****] or an electrode.

[0040] Moreover, according to the manufacture approach of the heterojunction transistor of this invention, and the heterojunction transistor 2nd Si(1-y) Gey film (0.05<=y<1) is formed on 1st Si(1-x) Gex film (0<=x<0.05), and since 1st Si(1-x) Gex film is 0.5nm or more thickness of 5nm or less The SiGe film with which the film dry area was controlled on the insulator layer is obtained, and the film which can be used as a low resistance base outgoing line can be obtained in spite of thin buffer thickness. Consequently, a SiGe base region can be produced now without a thick buffer layer, and non-choosing epitaxial growth can realize SiGe-HBT in which more nearly high-speed actuation is possible.

[Translation done.]

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CLAIMS

[Claim(s)]
[Claim 1] The buffer formation process which is the approach of forming the SiGe film on an insulator layer, and forms 1st Si(1-x) Gex film (0<=x<0.05) on said insulator layer, It has the main film formation process which forms 2nd Si(1-y) Gey film (0.05<=y<1) on said 1st Si(1-x) Gex film. Said buffer formation process The formation approach of the SiGe film characterized by forming said 1st Si(1-x) Gex film in [0.5nm or more / thickness] 5nm or less.
[Claim 2] The formation approach of the SiGe film which is the formation approach of the SiGe film according to claim 1, and is characterized by forming said 2nd Si(1-y) Gey film with the reduced pressure CVD method of 0.133Pa or more pressure range 1.33x104Pa or less at least.
[Claim 3] The process which forms an insulator layer on Si substrate with which it is the approach of manufacturing the heterojunction transistor which has the base region of SiGe, and the collector field was formed, The process which forms in said a part of insulator layer the window part which leads to said collector field, The SiGe film formation process which forms the field with which the outgoing line to a base electrode is presented on said insulator layer while forming the SiGe film in un-choosing on said window part and said insulator layer and forming said base region on a window part, It is the manufacture approach of the heterojunction transistor which is equipped with the process which forms the emitter region of Si on said base region, and is characterized by said SiGe film formation process forming said SiGe film by the formation approach of the SiGe film according to claim 1 or 2.
[Claim 4] Said SiGe film formation process is the manufacture approach of a heterojunction transistor that it is characterized by germanium presentation ratio y of said 2nd Si(1-y) Gey film being within the limits of 0.08<=y<=0.3 in the approach of manufacturing a heterojunction transistor according to claim 3.
[Claim 5] The collector field which is the heterojunction transistor which has the base region of SiGe, and was formed in Si substrate, An insulator layer with the window part which is formed on said Si substrate and leads to said collector field, The base region which is formed on said window part and consists of SiGe film, and the outgoing line which consists of SiGe film which was formed on said insulator layer and connected to said base region, It has the emitter region of Si formed on said base region. At least said outgoing line 1st Si(1-x) Gex film formed on said insulator layer (0<=x<0.05), It is the heterojunction transistor which is equipped with 2nd Si(1-y) Gey film (0.05<=y<1) formed on said 1st Si(1-x) Gex film, and is characterized by said 1st Si(1-x) Gex film being 0.5nm or more thickness of 5nm or less.
[Claim 6] Said 2nd Si(1-y) Gey film is a heterojunction transistor to which it is characterized by germanium presentation ratio y being within the limits of 0.08<=y<=0.3 in a heterojunction transistor according to claim 5.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the rough sectional view showing HBT in the formation approach of the SiGe film concerning this invention, the manufacture approach of a heterojunction transistor, and 1 operation gestalt of a heterojunction bipolar transistor.
[Drawing 2] In the formation approach of the SiGe film concerning this invention, the manufacture approach of a heterojunction transistor, and 1 operation gestalt of a heterojunction bipolar transistor, it is the sectional view showing the manufacture process to the 2nd SiGe film formation of HBT in order of a process.
[Drawing 3] In the formation approach of the SiGe film concerning this invention, the manufacture approach of a heterojunction transistor, and 1 operation gestalt of a heterojunction bipolar transistor, it is the sectional view showing the manufacture process from after the 2nd SiGe film formation of HBT to each electrode formation in order of a process.
[Drawing 4] In the formation approach of the SiGe film concerning this invention, the manufacture approach of a heterojunction transistor, and 1 operation gestalt of a heterojunction bipolar transistor, it is the SEM photograph in which the membrane formation condition of the 2nd SiGe film of HBT is shown.
[Drawing 5] It is the SEM photograph in which the membrane formation condition of the SiGe film of germanium presentation ratio 0.04 formed on SiO2 is shown.
[Drawing 6] It is the SEM photograph in which the membrane formation condition of the SiGe film of germanium presentation ratio 0.13 formed on SiO2 is shown.
[Drawing 7] It is the SEM photograph in which the membrane formation condition of the SiGe film of germanium presentation ratio 0.30 formed on SiO2 is shown.
[Drawing 8] It is the graph which shows the sheet resistance of the SiGe film at the time of changing the thickness of a buffer layer to 0-5nm.
[Description of Notations]
1 P-type Silicon Wafer (Si Substrate)
4 1st Collector Well (Collector Field)
5 2nd Collector Well (Collector Field)
6 The 1st SiO Two-layer (Insulator Layer)
7 Base Window Part (Window Part)
8 SiGe Film
9 1st Si(1-X) Gex Film
10 2nd Si(1-Y) Gey Film
11 Base Region
12 Base Outgoing Line (Outgoing Line)
16 Emitter Region
20 Base Electrode

[Translation done.]